NASA TECHNICAL
MEMORANDUM

NASA TM X-53548
November 21, 1966

NASA TM X-53548

INVESTIGATIONS OF MONOLITHIC INTEGRATED CIRCUIT FAILURES

by Kenneth W. Woodis
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ABSTRACT

This report presents the results of failure analysis performed on a group of monolithic integrated circuits obtained from industry. The devices tested were defective and had been rejected. The purpose of this study was to determine the most prevalent failure modes and/or causes of rejection of monolithic integrated circuitry, and to develop the capability of performing failure analysis of these devices.

The experiment showed the greatest causes of failure to be (1) bonding and (2) open or shorted aluminum interconnects. Other failure causes found were: too thin a layer of silicon step-up or step-down, poor adherence of aluminum to the silicon, failure to remove all surface contaminants, chipped dice, poor mask alignment, and defects in both the silicon material and the mask. It was determined that proper failure analysis could reveal over 90 percent of the failures encountered.

This analysis was performed under the support research task "Quality Control Requirements for Integrated Circuits, Project Number 125-21-03-1100".

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GLOSSARY

DIE - A single substrate on which all the active and passive elements of an electronic circuit have been fabricated utilizing the semiconductor technologies of diffusion, passivation, masking, photoresist, and epitaxial growth. A die (also called a chip) is not ready for use until it is packaged and provided with external terminals.

DICE - More than one die or chip.

FAILURE CAUSE - The nature of the actions which caused the failure mechanism phenomenon to occur.

FAILURE INDICATOR - The observed characteristic which tells that an item is defective.

FAILURE MECHANISM - The nature of the phenomenon which produced the failure mode discrepancy.

FAILURE MODE - The nature of the product discrepancy from which the observed failure indicating characteristic directly resulted.

INTEGRATED CIRCUIT - The Electronic Industries Association defines semiconductor integrated circuit as "the physical realization of a number of electronic elements inseparably associated on or within a continuous body of semiconductor material to perform the functions of a circuit".

MONOLITHIC - Also called "Single Stone", a single flat-surfaced die or chip of silicon onto which patterns may be drawn, scribed, diffused, etc.; the result being a single die or chip of material which has transistors, diodes, resistors, and capacitors formed on its surface.

SUBSTRATE - The physical material upon which a circuit is fabricated. Used primarily for mechanical support but may serve a useful thermal or electrical function.

THERMOCOMPRESSION BOND - A process involving the application of heat and pressure to a highly conductive fine wire in a metalization and/or external lead area to provide an electrical path for external stimuli or currents.

WAFER - A slice of semiconductor material from which dies or chips are formed.

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INVESTIGATIONS OF MONOLITHIC INTEGRATED CIRCUIT FAILURES

SUMMARY

A group of monolithic integrated circuits was obtained from industry. The circuits obtained were defective and had been rejected. These circuits were subjected to failure analysis to determine the most prevalent failure modes and/or causes of rejection, and to develop the capability of performing failure analysis of these devices.

The experiment showed the greatest causes of failure to be (1) bonding and (2) open or shorted aluminum interconnects. Other failure causes found were: too thin a layer at a silicon step-up or stepdown, poor adherence of aluminum to the silicon, failure to remove all surface contaminants, chipped dice, poor mask alignment, and defects in both the silicon material and the mask. It was determined that proper failure analysis could reveal over 90 percent of the failures encountered.

SECTION I. INTRODUCTION

The rapid application of microcircuitry to space systems prompted an investigation into the quality assurance aspects of integrated circuits. The investigation reported herein was directed toward the failure analysis of rejected devices from industry. This report presents no information which would indicate the reliability of the devices or which would indicate process yields. The study does, however, indicate that the majority of causes for rejection are quality failures as opposed to time dependent failures.

Note that the devices which were studied were rejected by industry, and no conclusion should be drawn as to the reliability of the particular devices.

A group of monolithic integrated circuits was obtained from industry. The devices supplied were "line rejects," i.e. they were defective and incapable of meeting specification requirements and were rejected by industry.

Individual items and their associated defects were not identified, therefore it became necessary to conduct complete failure analysis procedures within the capability of the laboratory.

The purpose of this study was to (1) determine, if possible, the most prevalent failure modes and/or causes of rejection of monolithic integrated circuitry, and (2) develop the capability of performing failure analysis of these devices.

SECTION II. TESTS PERFORMED

A. TEST ITEMS

The test items were monolithic integrated circuits manufactured and rejected by industry. It was decided at the beginning of the program that a better and more complete picture of failure modes could be obtained by procuring a group of known defective units which failed to meet specification requirements rather than procuring functional devices and inducing failures. This latter concept will be pursued at a later date. Thus, all the devices had some inherent defect and were supplied as such.

The items subjected to analysis are presented in table 1.

Table 1. Items Subjected to Analysis

TYPE	LOGIC FUNCTION	SAMPLE SIZE
DTL	NAND Gate	71
RTL	NOR Gate	66
DTL	Flip Flop	77
RTL	Flip Flop	75

The causes of rejection of the devices were not supplied by industry. This necessitated a complete analytical procedure. All devices were monolithic integrated circuits fabricated basically from a silicon structure and by diffusion techniques. The manufacturing processes and techniques are basically the same for all devices investigated and are fairly representative of those used by industry.

The interconnection system of these particular devices is an aluminum-aluminum system and an aluminum-gold system. These particular systems consist of aluminum thin film deposited on the silicon. Gold or aluminum leads are then bonded to the aluminum thin film usually by thermo-compression bond techniques. The silicon chip is generally enclosed in a ceramic hermetically sealed package to protect the devices from contamination.

B. FAILURE ANALYSIS PROCEDURE

The basic approach to evaluation and analysis of the devices is shown in figure 1. Note that a maximum of nondestructive testing was performed prior to performing any destructive tests.

C. VISUAL EXAMINATION

Visual examination with the unaided eye was performed upon receipt of the components. Additional microscopic inspection at 30X was performed in an effort to detect gross defects such as missing leads, cracked cases, and improper index marking.

D. PERFORMANCE TESTS

Performance tests were conducted on the devices which were susceptible to this type of test. Several devices exhibited missing functional leads; therefore a complete functional test could not be performed.

Electrical functional tests were selected in such a manner as to verify the operational characteristics of the units. Verification of logic functions and status parameter tests were performed on a DC Integrated Circuit Tester.

SECTION III. DETERMINATION OF FAILURE INDICATORS

Subsequent to the electrical parameter measurement and nondestructive tests, the case of each unit was carefully removed to facilitate internal investigation. The monolithic chip and all interconnections were then accessible for microscopic observation; and, such manufacturing process deficiencies as inadequate lead bonding, improper handling, erroneous registration, and improper index markings could be easily observed.

SECTION IV. RESULTS

A. DTL NAND GATE

The results of the visual inspections and electrical tests are shown in Table II. These tests primarily verified that the units were defective and provided the failure indicator from which subsequent analysis proceeded. Note that 14 of the units appeared to be non-failures.

Microscopic examination of the opened units revealed the failure mechanisms and causes as shown in Table III. During this phase of the investigation it became apparent that many of the devices that were thought to be DTL NAND were in reality DTL power NAND or a circuit that had 1126, which bore no resemblance to the original circuit printed on the die. This was discovered initially by observation of the chip code and subsequently verified by electrical tests. Since the electrical characteristics of the three types of devices are different, and the devices were labeled internally, they were rejects on an electrical parameter test basis.

Note that the majority of defective units can be categorized as quality failures, which are those failures caused by human error and/or

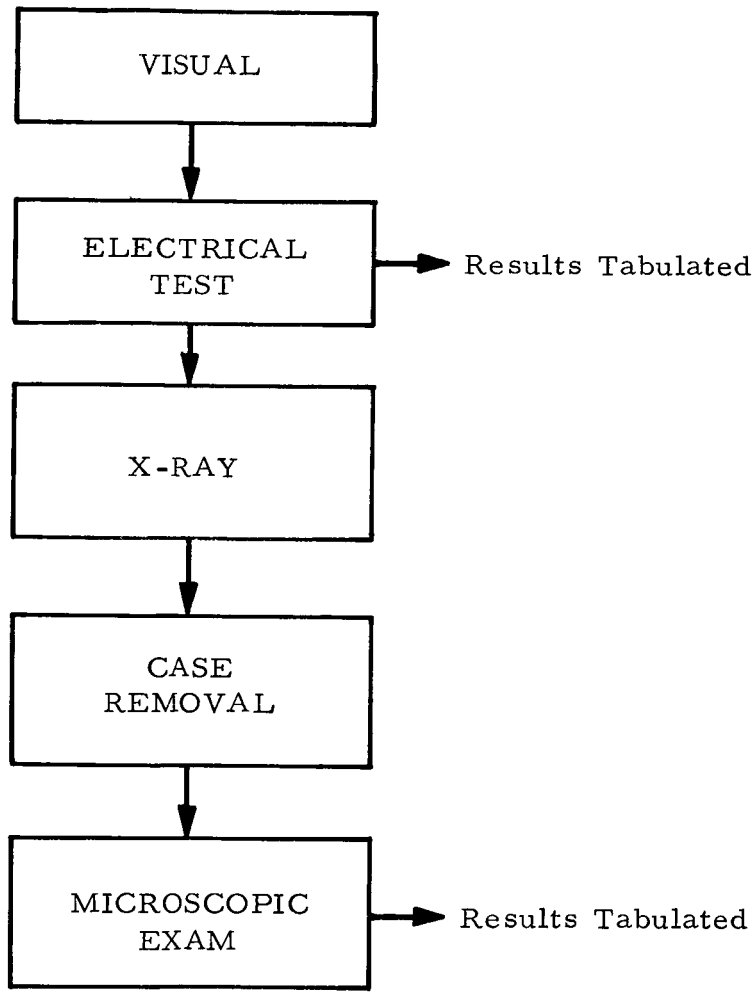

Figure 1. Failure Analysis Procedure

Table II. Determination of Failure Indicators For DTL NAND Gates

DEFECTS	NUMBER OF UNITS	METHOD	
		DC TEST	MICROSCOPIC INSPECTION
Input either Shorted or Open	4	4	1**
Transistor Open	7	7	2**
Transistor Shorted	11	11	5**
Output Out of Tolerance	23	23	0
Wrong Circuit in Capsule (1126)	19	0	19
Leaking Transistor*	15	15	0
Unit appeared To Be Good	--	14	43

* DC Test of units with 1126 circuit made unit appear to have leaky transistor.

** Verification of DC Test made by Microscopic Inspection.

Table III. Failure Mechanisms and Causes

UNIT NO.	TYPE	FAILURE INDICATOR (DC TESTS)	FAILURE MODES (VISUAL INSEPCTION)	FAILURE MECHANISMS	FAILURE CAUSE
1	DCTL Power NAND	Outputs Always "True"	Unknown Nothing Visible	Probably Die not Properly Formed	Quality Control
3	1126	Output Voltages Not Stable	Wrong Circuit	Improper Packaging	Improper Packaging
6	DTL Power NAND	Outputs Always "False"	Unknown Nothing Visible	Probably Die not Properly Formed	Quality Control
10	DTL Power NAND	One Output Always "True" Other Always "False"	Open and Shorted Transistors	Die Scarred	Improper Tooling
24	DTL Power NAND	One Output Always "False" Other Normal	Shorted Transistor	Die Chipped	Improper Tooling
38	DTL Power NAND	Output Voltages Not Stable and Input Directly Connected	Transistor Failing To Saturate and Diode Shorted At Input	Die Scarred	Improper Tooling
46	DTL Power NAND	One Output Always "False" and The Other Out of Tolerance	Unknown Nothing Visible	Probably Die not Formed Properly or Die Contaminated	Quality Control
60	DTL Power NAND	Both Outputs Out of Tolerance	Unknown Nothing Visible	Probably Die not Formed Properly or Die Contaminated	Quality Control

improper quality control. This category of failure includes (a) improper process tool use resulting in scarred, chipped, and cracked substrates, (b) improper packaging such as erroneous registration and misindexing, and (c) poor lead bonding.

Scarred dice are shown in figures 2 and 3. Note the gouging of the die surface due to operator mishandling. Figure 2 shows a short caused by smearing of aluminum. This short has completely eliminated the function of one of the transistors within the circuit. Figure 3 shows an open circuit due to a tool scratch across aluminum interconnects.

Figure 4 shows a chipped die causing an open circuit. Note that the silicon is completely removed from a contact. Obviously extremely rough treatment was experienced.

Figure 5 depicts a poorly bonded lead. The bond is a thermocompression stitch type, and it is obvious by the tooling impressions that at least three attempts were made to accomplish this bond.

B. RTL NOR GATE

The results of the visual inspection and electrical tests are shown in Table IV. It was assumed that the units were rejected for improper indexing. Note that 100 percent of the units had the mark on the case in the upper right-hand corner. Improper indexing was established by removing the case of a unit and tracing the circuit. Although the erroneous indexing was discovered, the analysis proceeded as if the units were properly indexed. This discrepancy was considered during the test. The electrical test indicated that all units were well within tolerance limits and performed correctly.

Microscopic examination of the opened units revealed several types of probable failure mechanisms. Since there were no failure indicators one can assume that the mechanisms might manifest themselves as failures at some future time. Note that a majority of the units had such mechanisms as mentioned in the DTL NAND gate description. These mechanisms were caused mainly by improper quality control. This category includes (a) improper process tool use resulting in scarred, chipped, and cracked substrates, (b) poor cleanup of etchant,

Table IV. Results of Visual Inspection and Electrical Tests

NUMBER OF UNITS	FAILURE INDICATOR DC TESTS	FAILURE MODES (VISUAL INSPECTION)	FAILURE MODES	FAILURE CAUSE
31	None	None	None	None
19	None	Possible Future Short or Opens	Die Scarred	Improper Tooling
9	None	Possible Future Shorts or Opens	Crack in Substrate	Improper Handling
5	None	Possibility of Item Being Out of Tolerance	Resistor Pattern not Linearly Symmetric	Quality Control
4	None	Values of Elements Changing	Etching Process Still Continuing	Cleanup not Complete
2	None	Possibility of Item Being Out of Tolerance	Depth of Deposited Resistor not Uniform	Quality Control
1	None	Possibility of Future Opens or Shorts	Substrates Chipped	Improper Handling

and (c) poor lead bonding. A scarred die similar to those discussed earlier is shown in figure 6. The arrow points to a smear which could cause a poor thermocompression bond, resulting in an intermittent failure. As in DTL NAND, these scars are also due to operator mishandling. Figure 7 shows inconsistencies in deposit thickness, which are probably due to improper control of deposition process.

When all of the etchant is not cleaned off the dice, or moisture is allowed to contact the dice, the process of delayed etching takes place as shown in figure 8. Another type of chemical process, not pictured here, is a metallic interaction between gold and aluminum. This causes a highly resistive compound called purple plague. The interaction is accelerated by high temperature.

A crack in the substrate at a transistor can be catastrophic but is not as serious in the area of passive elements. This phenomenon is seen in figures 9 and 10; the electrical tests of these units showed them to be good.

Figures 11 and 12 show passive elements that were not linearly symmetric, which would cause variations in the values of resistance in the item. These variations are caused by improper processing of diffusion masks.

C. DTL FLIP FLOP

The results of the different phases of the analysis were correlated and then tabulated in Table V. Note that 66 of the units had the same failure indicator, and, of the 66, 44 had the same failure mode.

In almost every instance the microscopic examination yielded a failure mode for each indicator. Some of the modes found were: (1) etchant on die, (2) interconnecting lead bonds not completely on pads, and (3) leads that were open or shorted. The failures were further broken down into indicators, modes, mechanisms, and causes in Table VI.

Figures 13 and 14 present errors caused by a faulty mask or mask positioning. Notice that the aluminum lead in the middle of figure 13 was covering less than half of the bonding pad. The two diodes in figure 14, which have a common lead, had each end of this lead bonded to two layers of different heights; thereby shorting the diode to a lower layer of the circuit.

Table V. Determination of Failure Indicators For DTL Flip Flop

FAILURE INDICATOR	NUMBER OF UNITS WITH DEFECTS	FOUND BY DC TEST	VERIFIED BY MICROSCOPIC INSPECTION
Input Gates not Effecting Correct Output	66	66	65
Output Having Low Voltage Level	4	4	---
Input Appeared Open or Shorted	5	5	2
No Output	2	2	---
Output Triggered in Wrong Place	2	2	---

Table VI. Failure Classification

NUMBER OF UNITS IN CATEGORY	FAILURE INDICATOR	FAILURE MODES	FAILURE MECHANISM	FAILURE CAUSE
47	Input Gates not Effecting Correct Output	Lead Bonded to Two Different Layers on Die	Circuit Elements Improperly Formed	Faulty Circuit Masking
11	Input Gates not Effecting Correct Output	Open and Shorted Leads	Die Scarred	Improper Handling of Die
8	Input Gates not Effecting Correct Output	Open and Shorted Leads and Element Characteristics Changed	Etchant on Die	Cleanup of Die not Complete
5	Input Open or Shorted	Open and Shorted Leads	Etchant on Die	Cleanup of Die not Complete
1	Input Open or Shorted	Part of Circuit Detached From Rest	Crack in Die	Improper Scribing of Die

There were several mechanisms which indicated improper handling of the die. Figure 15 shows a die that was cracked through a transistor and a resistor area. Figure 16 shows damage that was probably caused by improper use of a microprobe or a tool used to position the die.

Another serious problem found was the double bonding of input-output leads. Figure 17 shows a lead that was broken off and another bonded next to it, while figure 18 shows a bond in which the aluminum and part of the insulation below it were torn away; thereby shorting the pad to the lower layers of the die.

The last series of pictures presents units which had been subjected to alumina hydration and chemical degradation. Figure 19 clearly shows a case where moisture or the etchant used on the die was not completely removed. Figure 20 presents the case where an etchant has been allowed to contact an aluminum lead thereby eating the aluminum lead in half. Figure 21 shows alumina hydration taking place on the aluminum.

D. RTL FLIP FLOP

It was discovered by the electrical test that only three of these units were RTL flip flops; the rest were either counter adapters or RTL gates. All of the RTL flip flop units were failures, but the counter adapters and RTL gates were shown by the electrical tests to be good. No analysis was performed on these units because there were not enough of the RTL flip flops to reveal any trends, and the good units were saved for future use in accelerated life tests.

SECTION V. ANALYSIS OF RESULTS

It was concluded from the analysis of the DTL NAND gate that:

31.0% Failed because of improper tooling
32.4% Failed because of improper packaging
26.8% Failed because of improper circuit values
19.7% Appeared to be good

If these percentages were totaled, the sum would be more than 100 percent. This would be true because some units had more than one failure cause.

It was concluded from the analysis of the RTL NOR gate that:

100 percent failed because of misindexing, and the following percentages had these possible failure mechanisms.

46.8%	Appeared to be good
28.8%	Had scarred dice
13.6%	Had cracked substrates
7.5%	Had linearly unsymmetric resistor patterns
6.0%	Had etching damage
3.0%	Had non-uniform resistor thickness
1.5%	Had chipped dice

Since 100 percent of the units failed because of misindexing, any of the other possible failure mechanisms were anticlimactic.

When a nonreject (out of our own supply) RTL NOR gate unit was opened and visually inspected under the microscope, it was discovered that the type of wire used from the die to the leads had been changed. The RTL NOR gate rejects had gold wires and the good unit had aluminum. The change was probably made to eliminate purple plague. No purple plague was found on the gold aluminum bonds, however.

It was found from the analysis of the DTL flip flop that:

6.5%	Appeared to be good
7.8%	Failed because etchant had opened, or foreign matter had shorted out leads
85.7%	Failed because either one or both of the input gates were disabled.
Total 100.0%	

NOTE: The 7.8% were not part of the 85.7% group.

The 85.7% group can be broken down into the following percentages of that group alone:

71.3%	Were caused by faulty masks
16.7%	Were caused by faulty handling
12.0%	Were caused by poor cleanup
Total 100.0%	

When the unit pictured in figure 20 was inspected, it was decided that a more extensive analysis of the affected aluminum leads was in order. This would involve either using an electron microscope analysis or actually scraping off some of the affected area and using x-ray diffraction methods to analyze the compound; however, this would be out of our present scope of work and was not performed.

SECTION VI. CONCLUSIONS

This experiment confirmed that the greatest cause of failure was bonding. It was shown by microscopic examination that a very high percentage of internal leads had been bonded two or three times to the substrates land patterns before a good connection had been made. This could only be detected on the aluminum to aluminum systems. The gold to aluminum systems could and probably would, with temperature and age, exhibit purple plague, an intermetallic formation which is high resistive to electron flow.

The second greatest offenders were open and/or shorted aluminur interconnects. The most frequent of these were the errors caused by human handling. Persons handling these monolithic chips as they would a transistor, with tweezers, caused complete opens or shorts by smear ing the aluminum interconnects. Frequently these scrapes or smears will not cause a complete open or short but will with time cause intermittent or complete failures. These are the most frustrating of all failures because they are virtually undetectable by electrical functional testing.

Other errors which lead to open or highly resistive aluminum interconnects are too thin a layer at a silicon step-up or stepdown, poor adherence of aluminum to the silicon, and failure to remove all surface contaminants which will cause sublimation, as corrosion of the aluminum.

Other failure modes detected were chipped dice, poor mask alignment and defects in both the silicon material and the mask, all of which could cause electrical shorts or opens internal to the silicon.

As is clearly seen, most of these faults, whether detectable by electrical tests or not, could be clearly found if a microscopic examination occurred after bonding the silicon die to the header. Therefore, electrical testing and microscopic examination prior to the attachment of the header to facilitate a hermetic seal could reveal over 90 percent of the failures encountered.

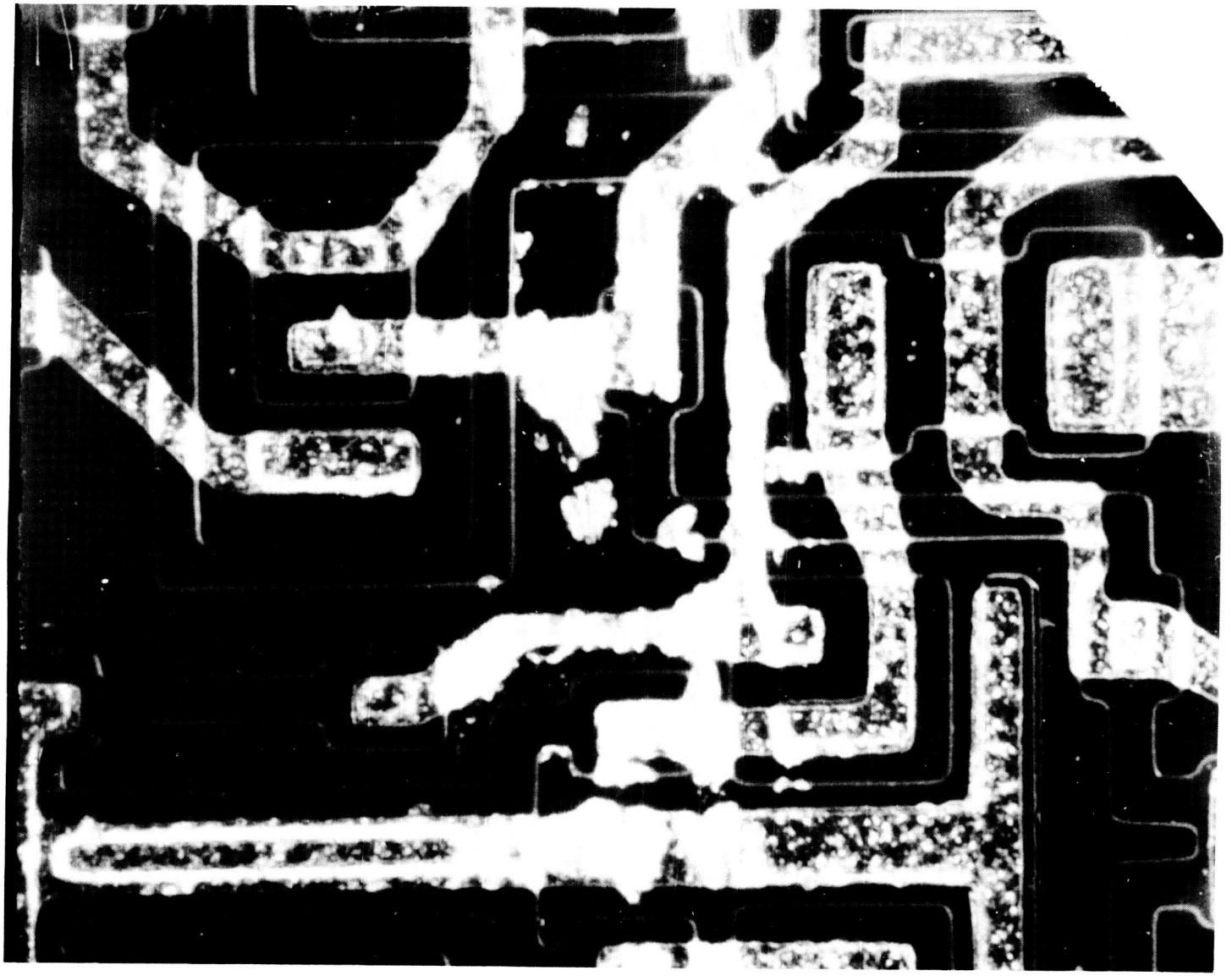

Figure 2. A Short Caused by Smearing of Aluminum

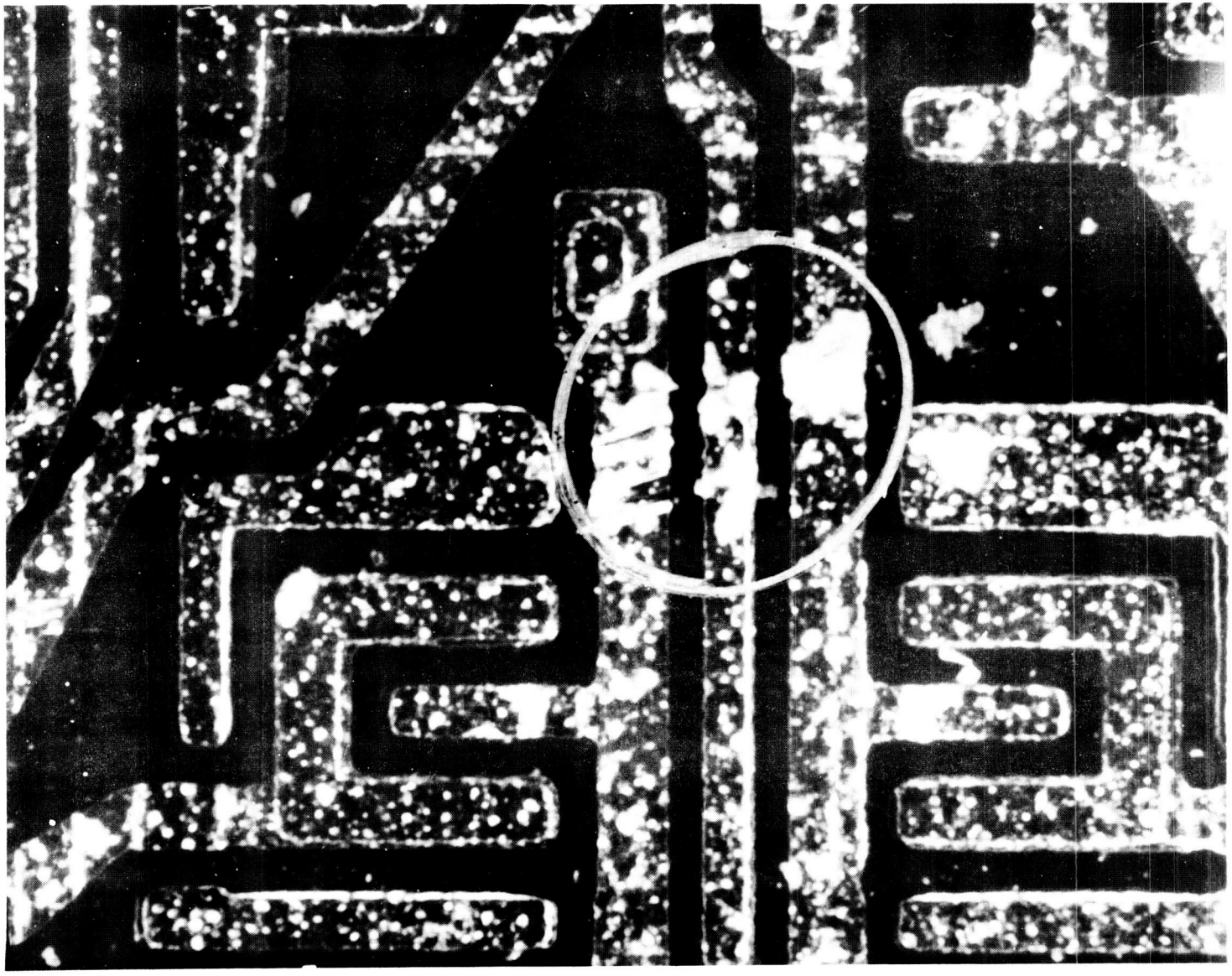

Figure 3. An Open Circuit Caused by a Tool Scratch Across Aluminum Interconnects

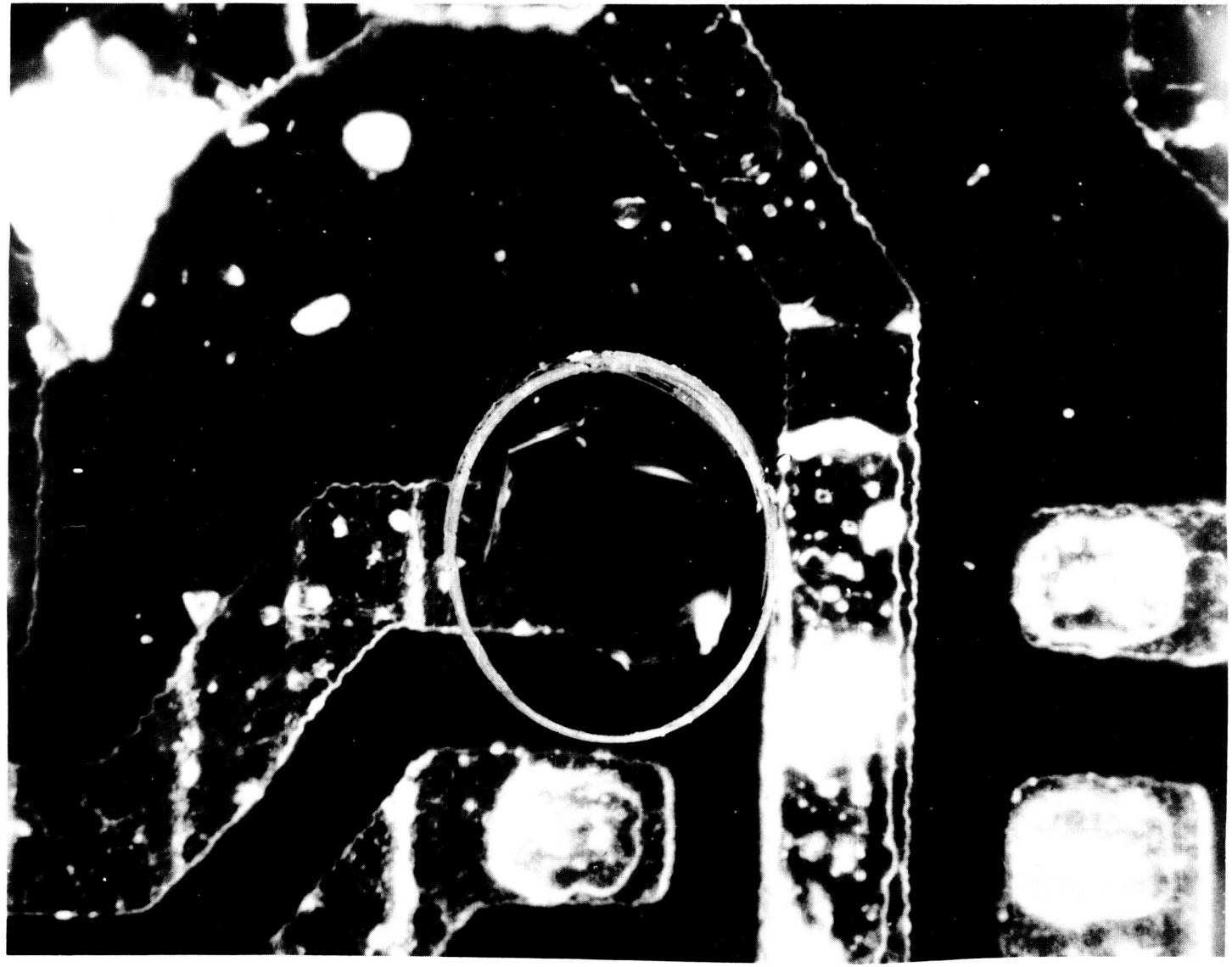

Figure 4. An Open Circuit Caused by a Chipped Die

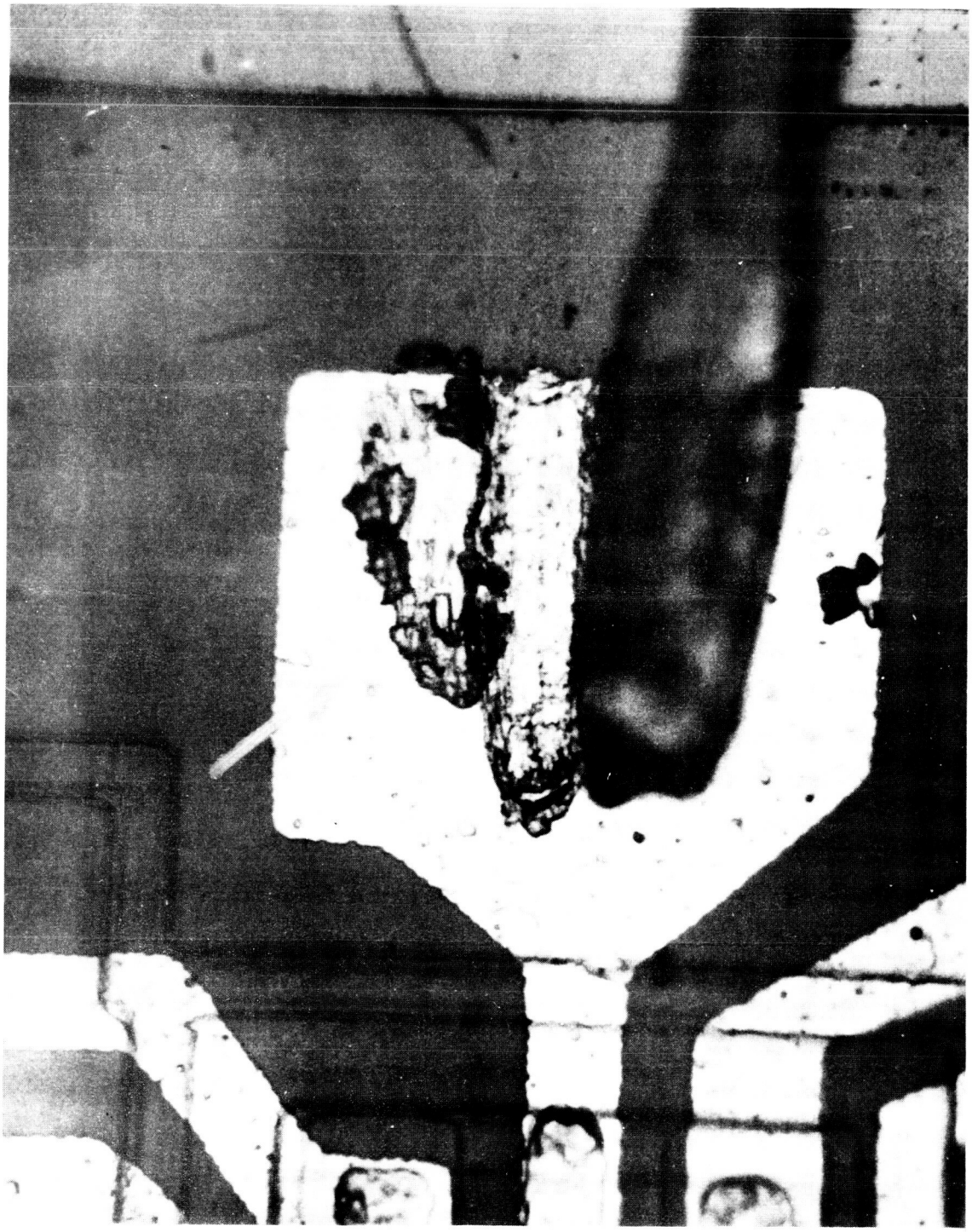

Figure 5. A Poorly Bonded Lead

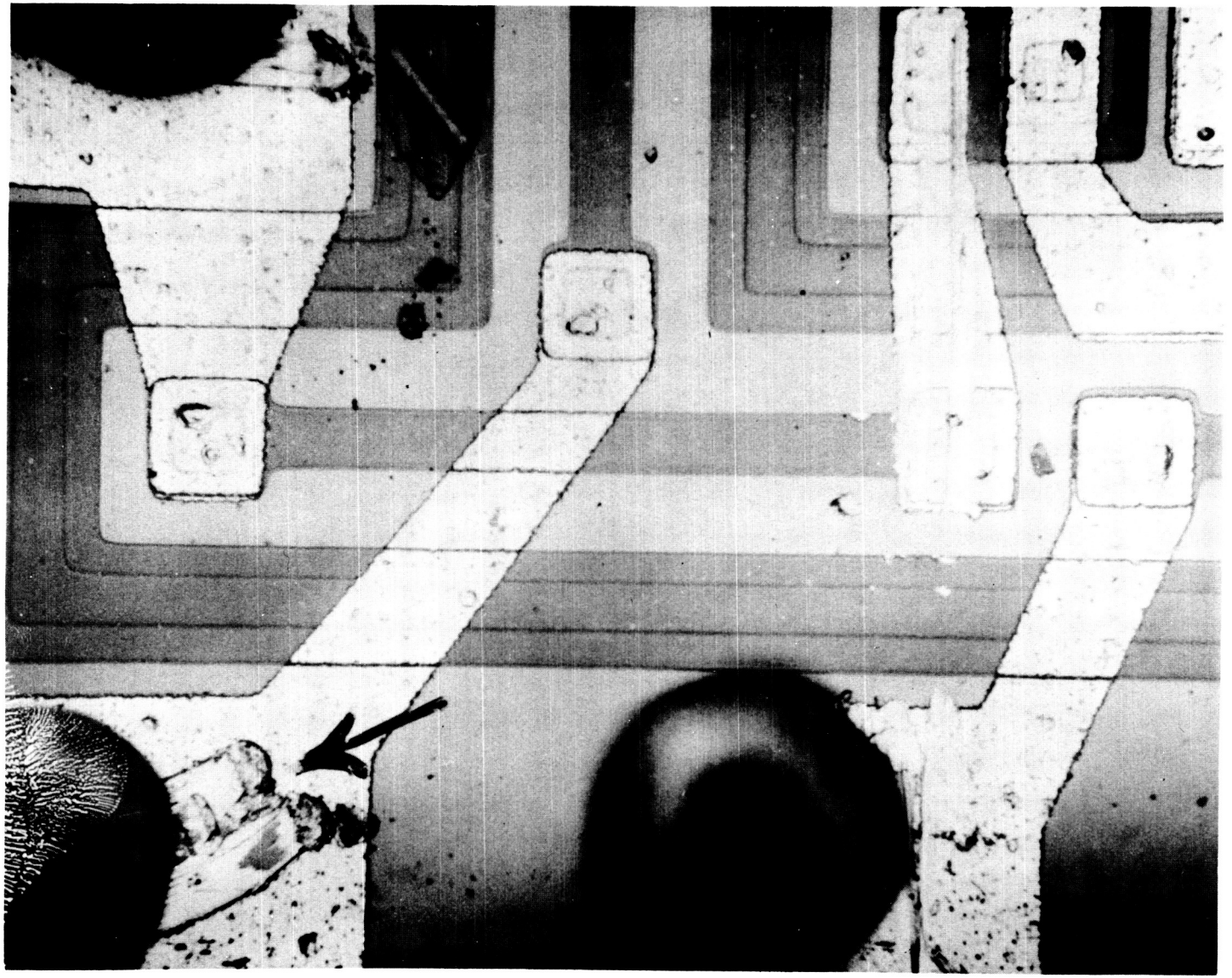

Figure 6. A Smear Which Could Cause a Poor Thermocompression Bond

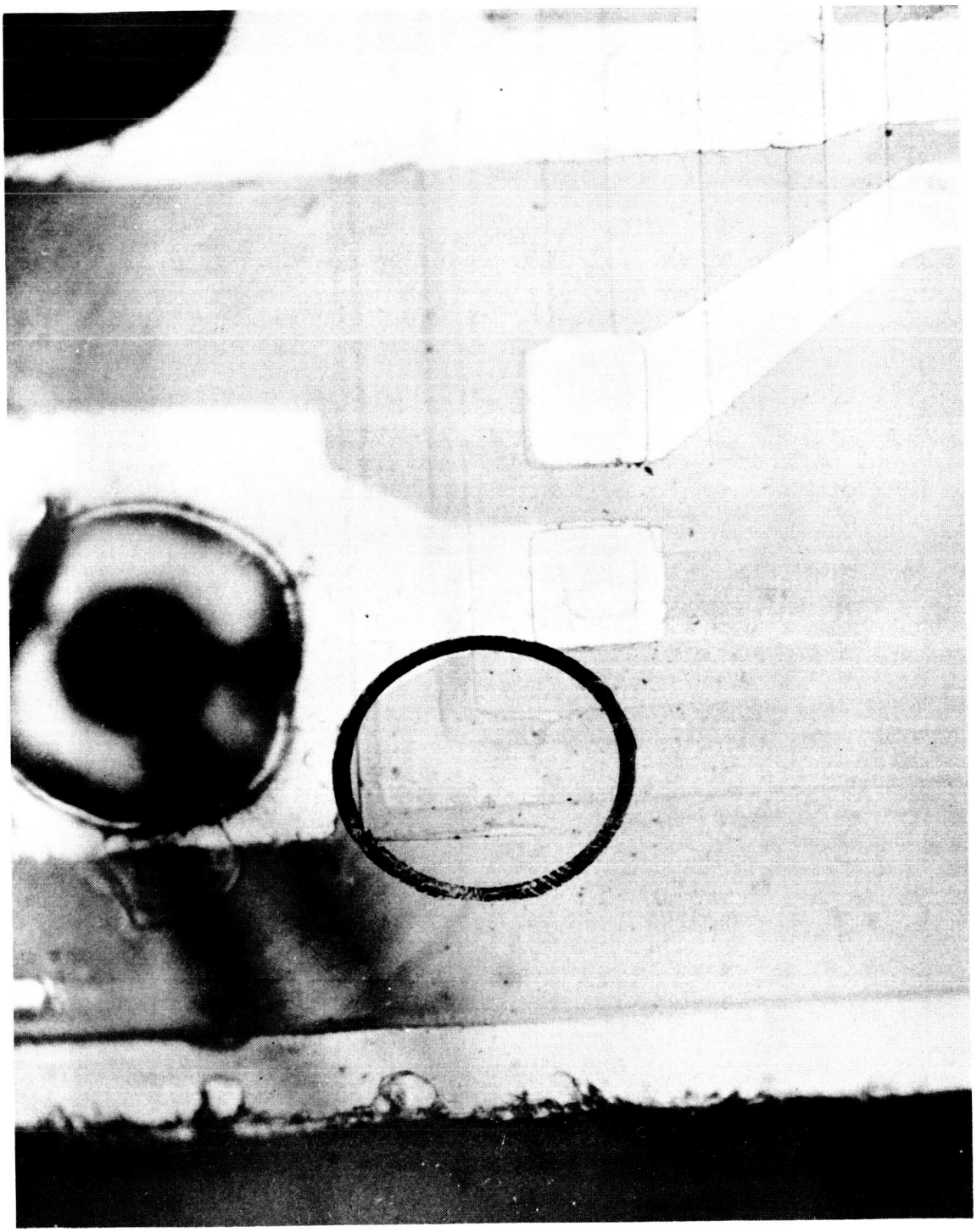

Figure 7. Inconsistencies in Deposit Thickness

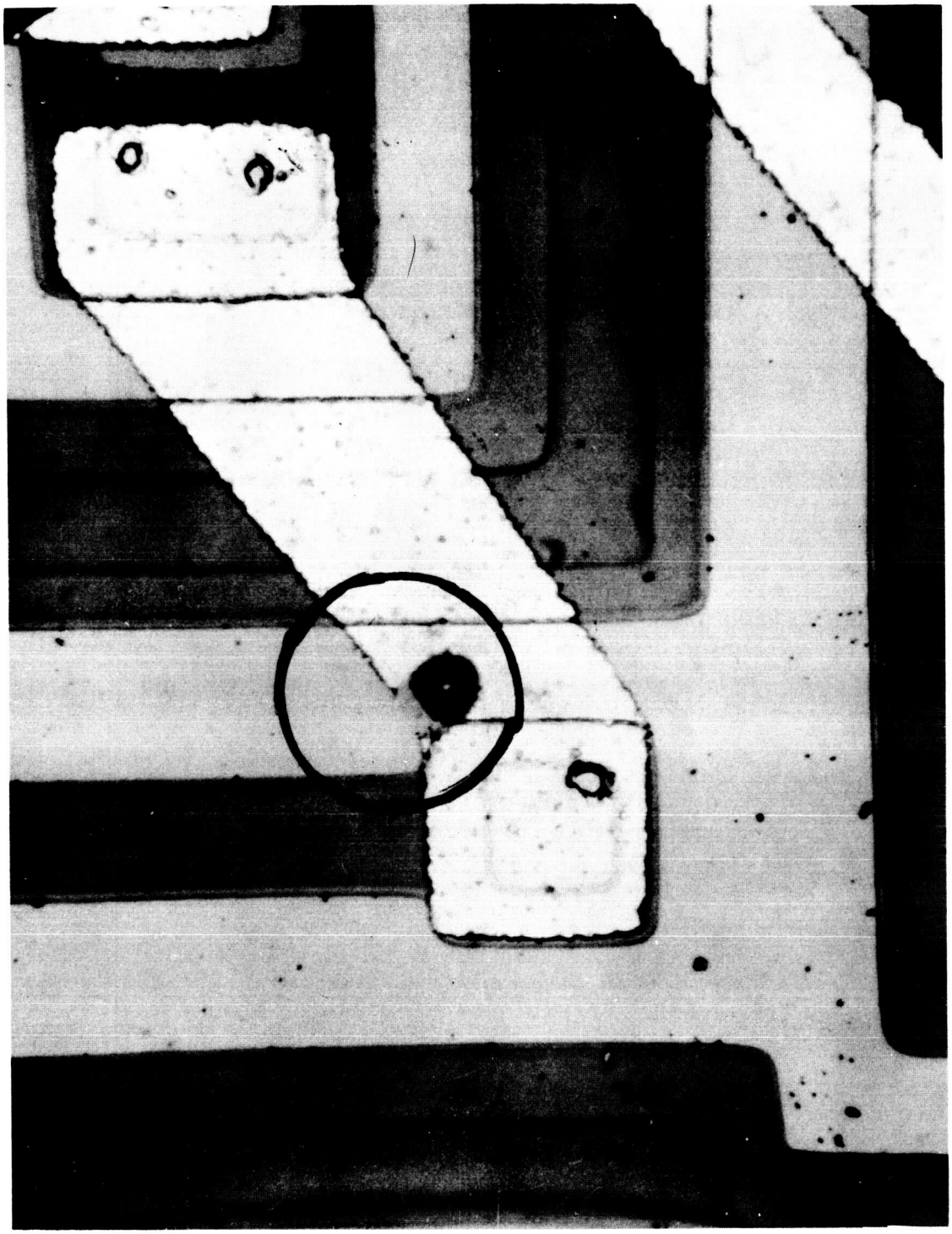

Figure 8. Delayed Etching

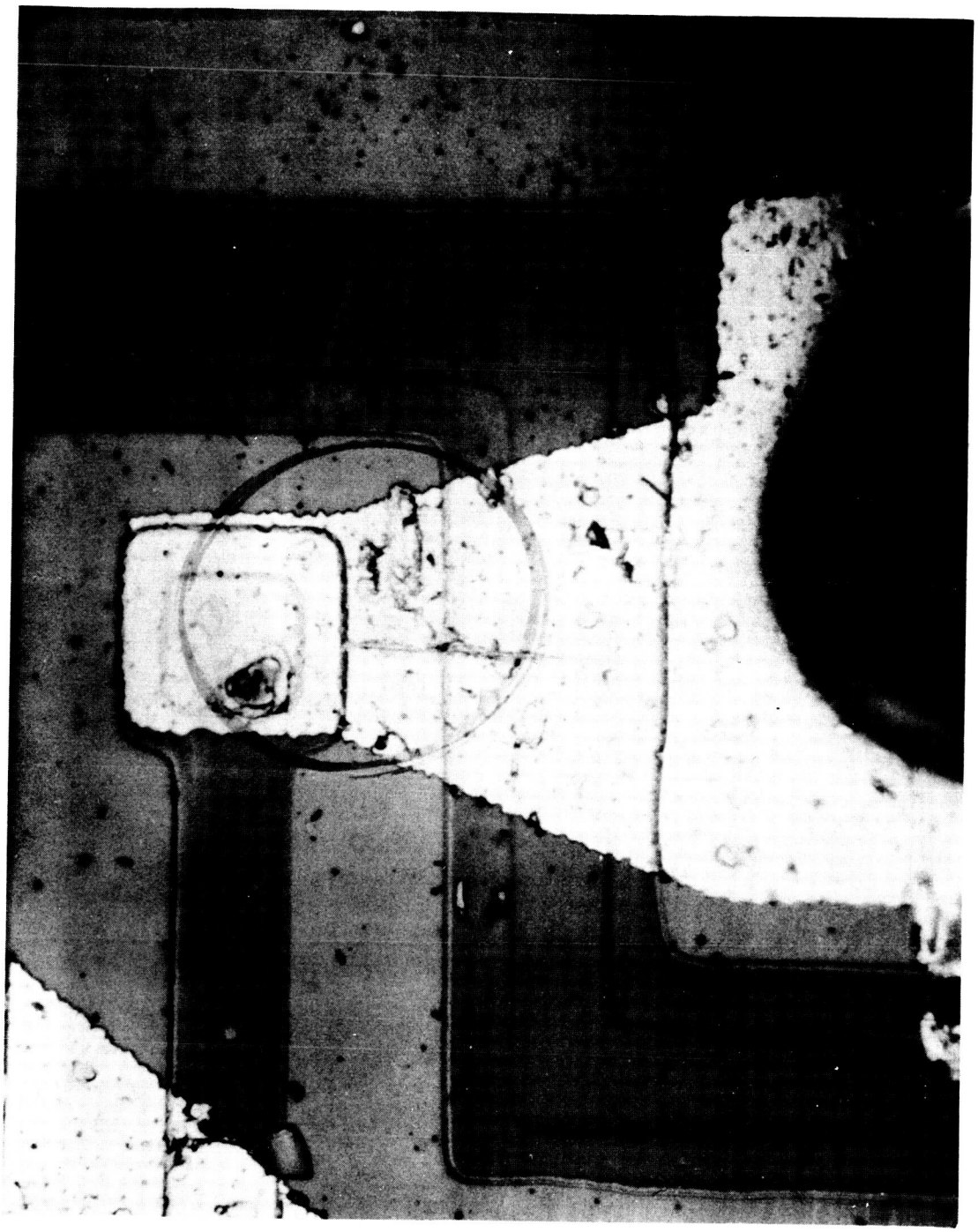

Figure 9. A Crack in Substrate

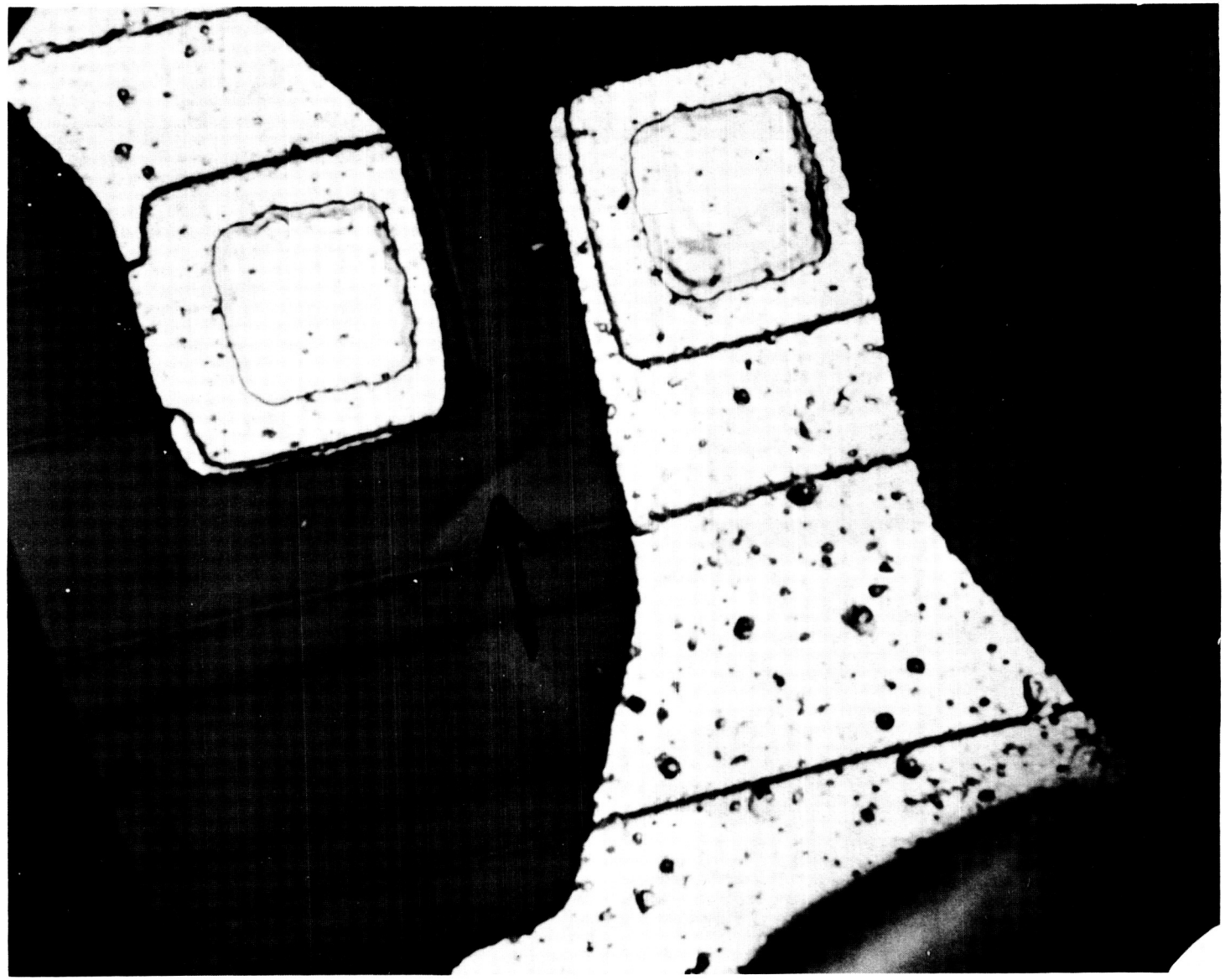

Figure 10. A Functioning Unit Despite Cracked Substrate

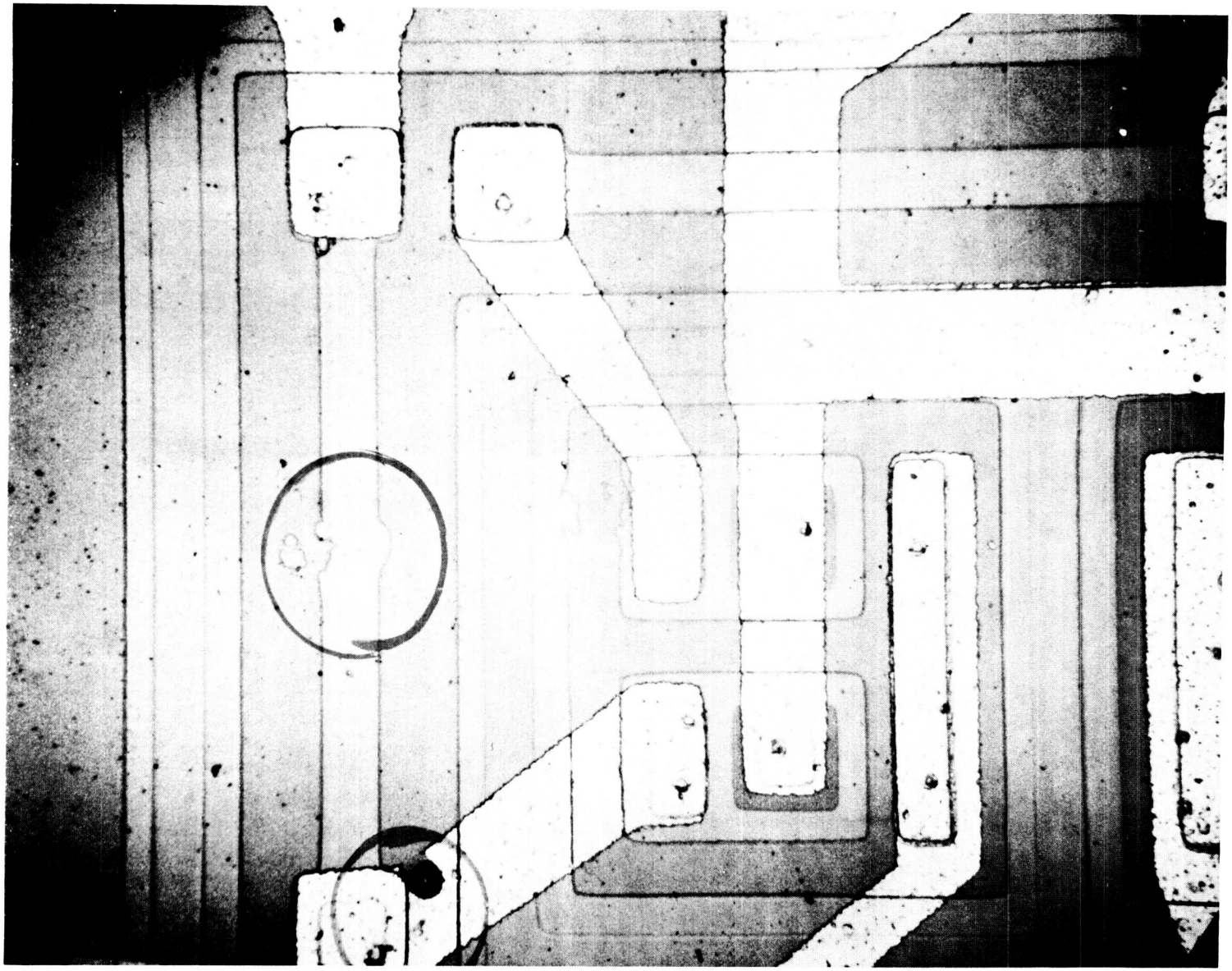

Figure 11. Variations Resulting From Improper Processing of Diffusion Masks

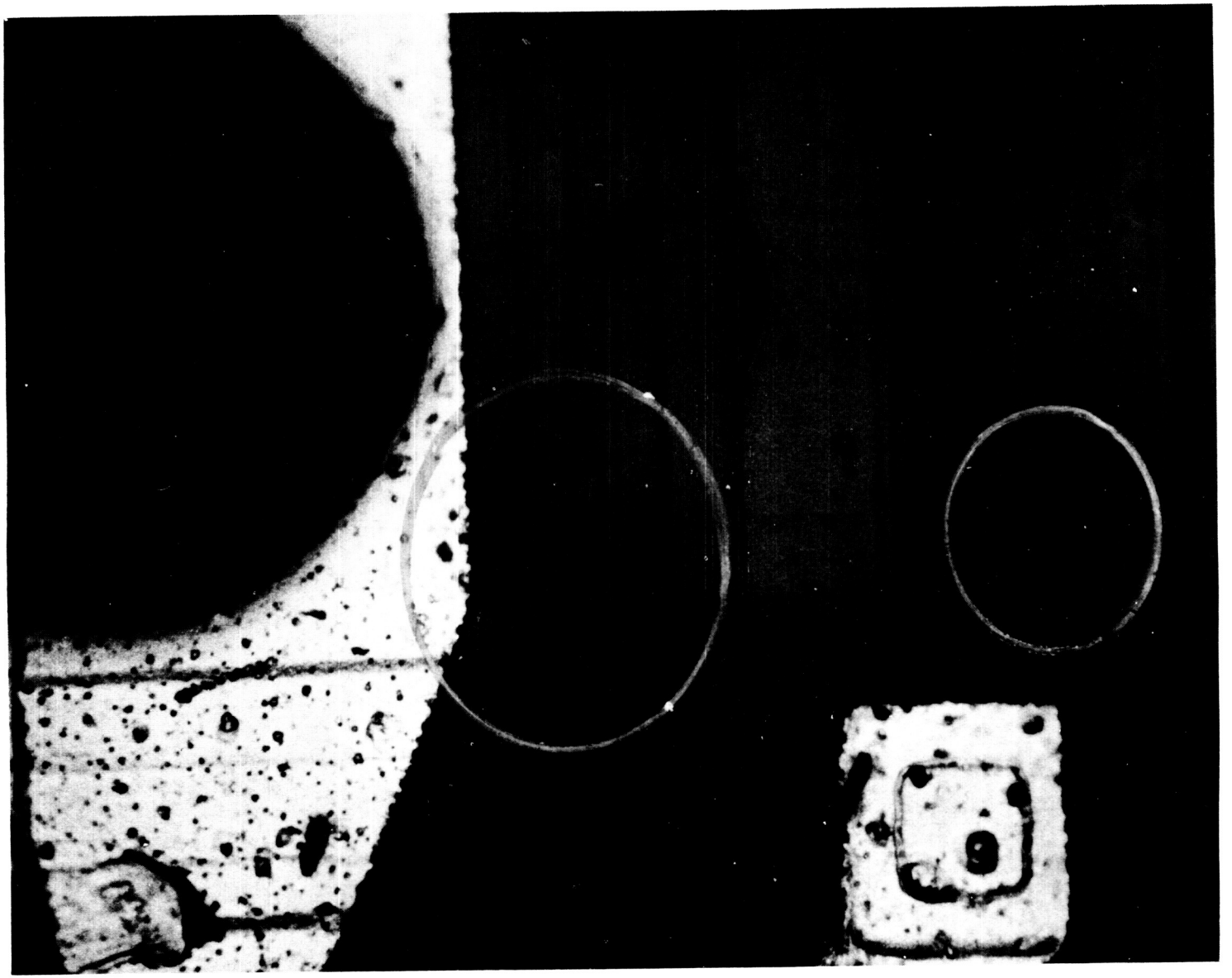

Figure 12. Values of Resistance Altered by Improper Processing of Diffusion Masks

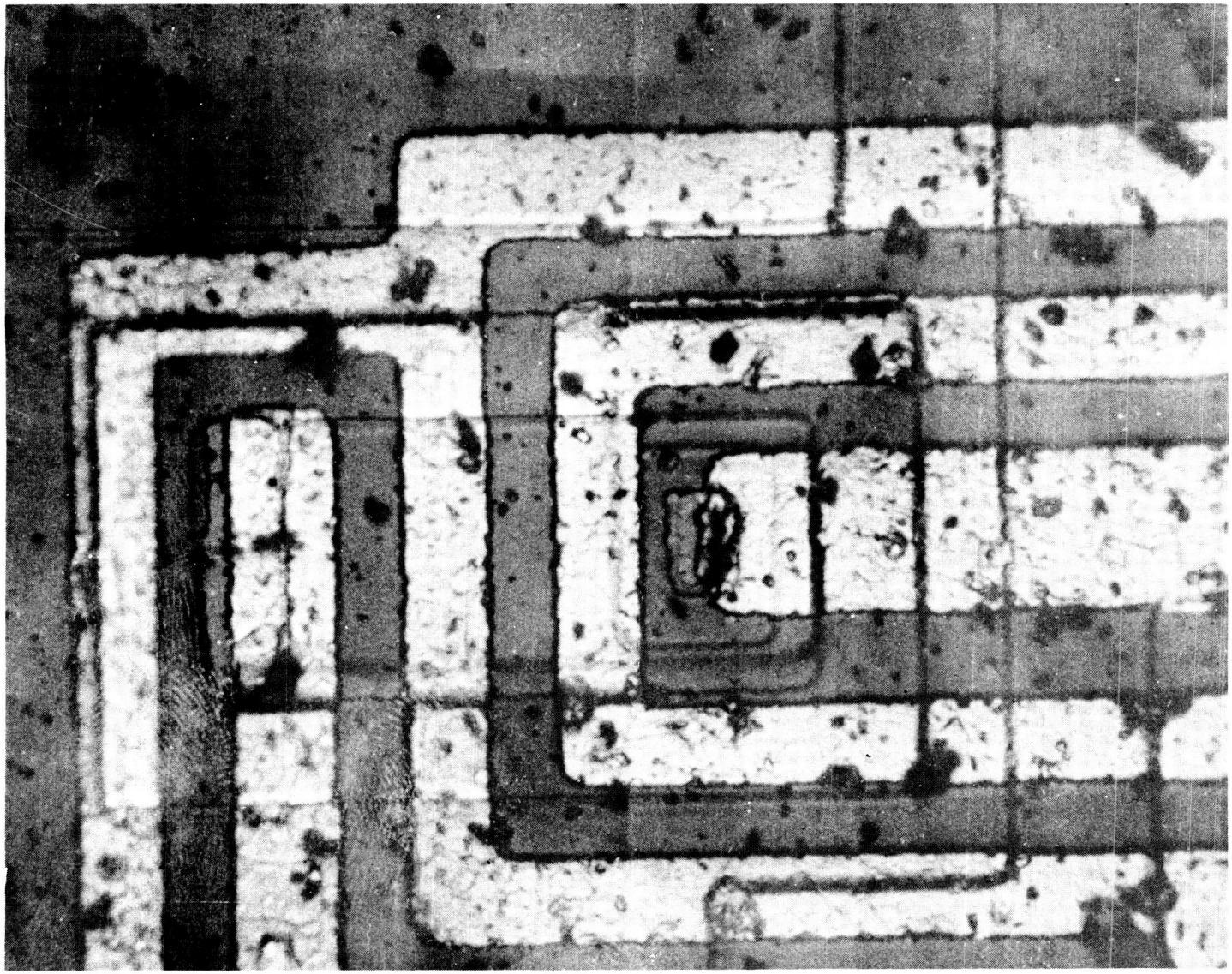

Figure 13. Aluminum Lead Covering Less Than Half of the Bonding Pad

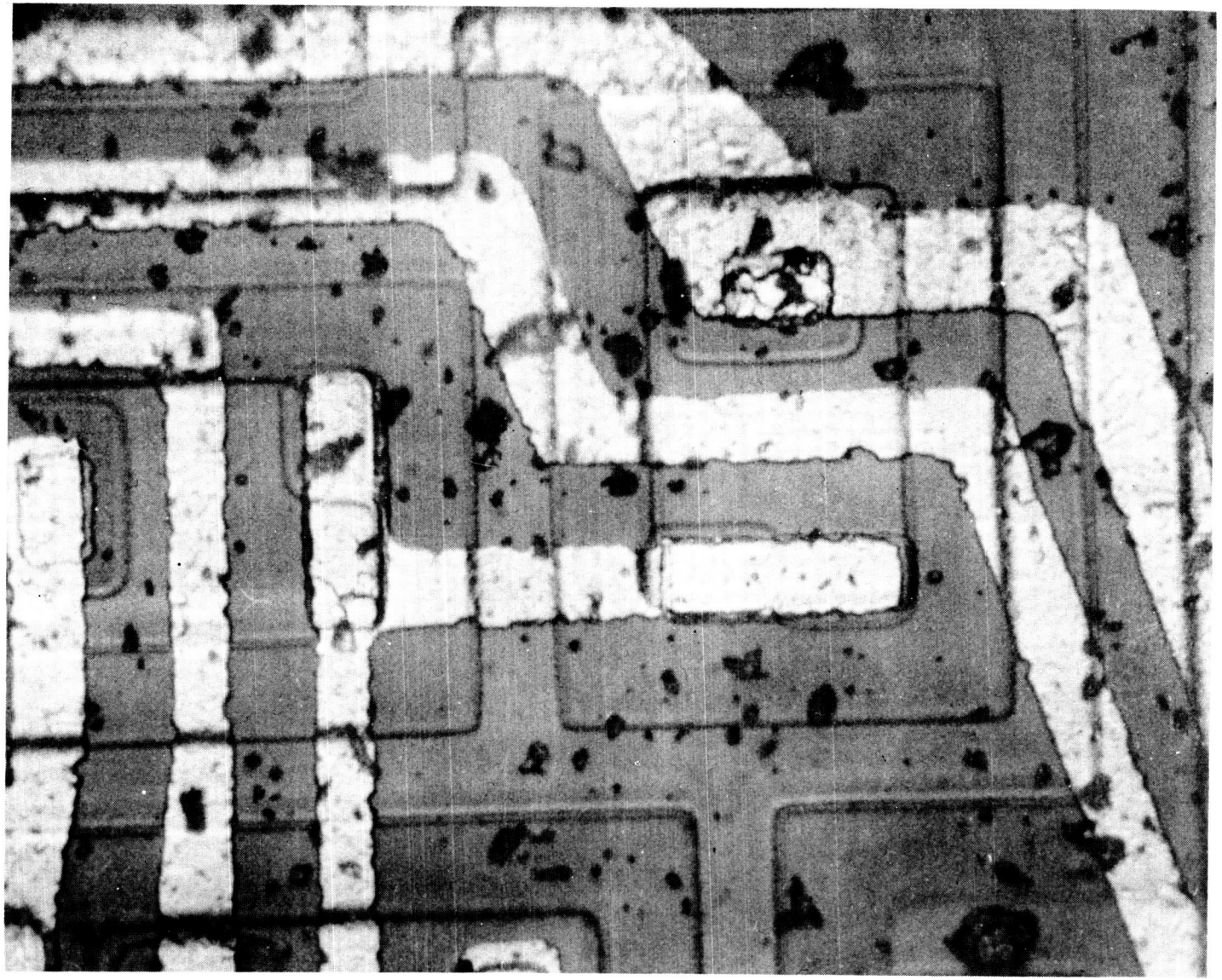

Figure 14. A Short Caused by Faulty Mask Positioning

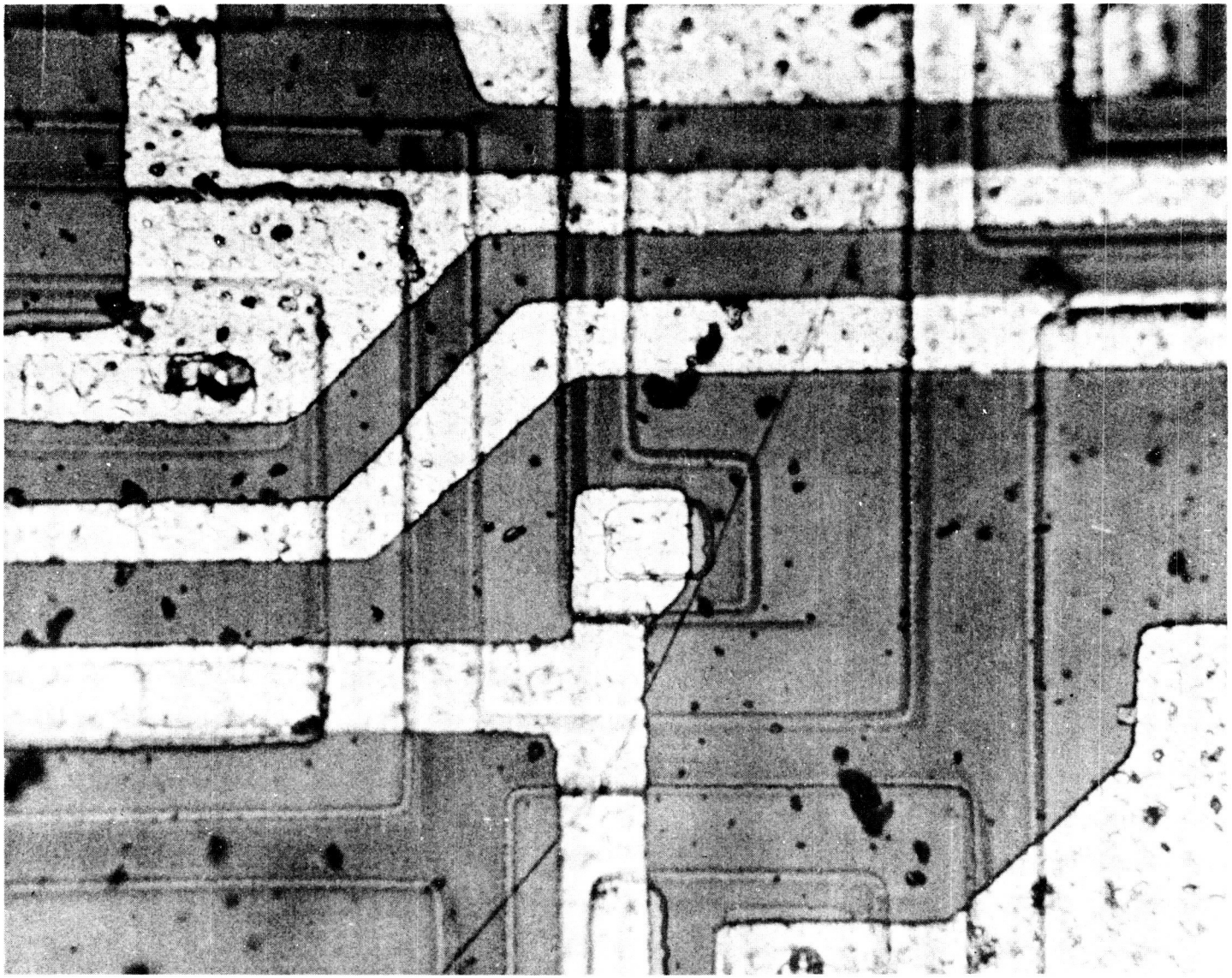

Figure 15. A Die Cracked Through a Transistor and a Resistor Area

Figure 16. Damage Caused by Improper Use of a Microprobe or a Tool Used to Position the Die

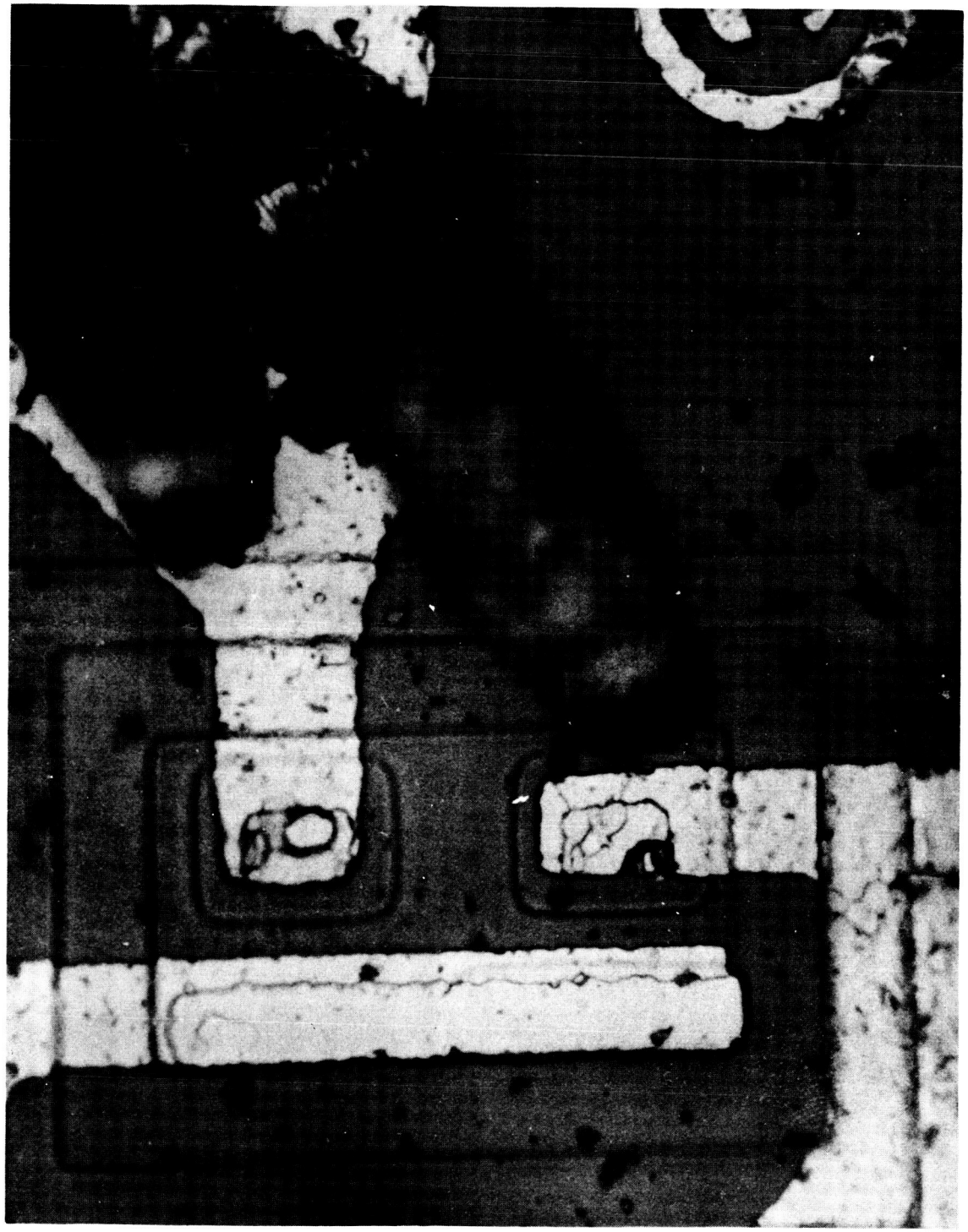

Figure 17. Double Bonding of Input-Output Leads

Figure 18. Short Caused by Double Bonding

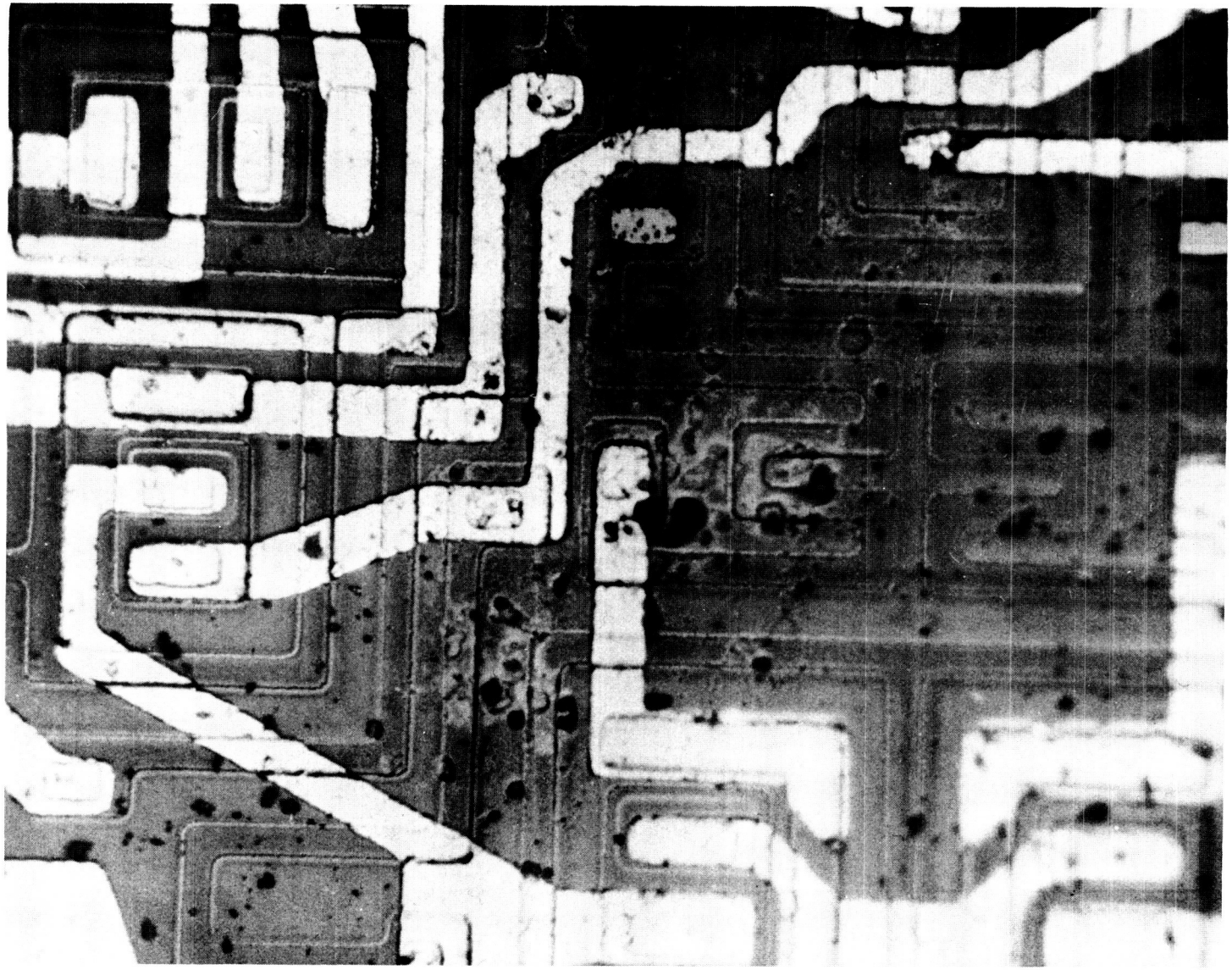

Figure 19. Etchant on Die Not Completely Removed

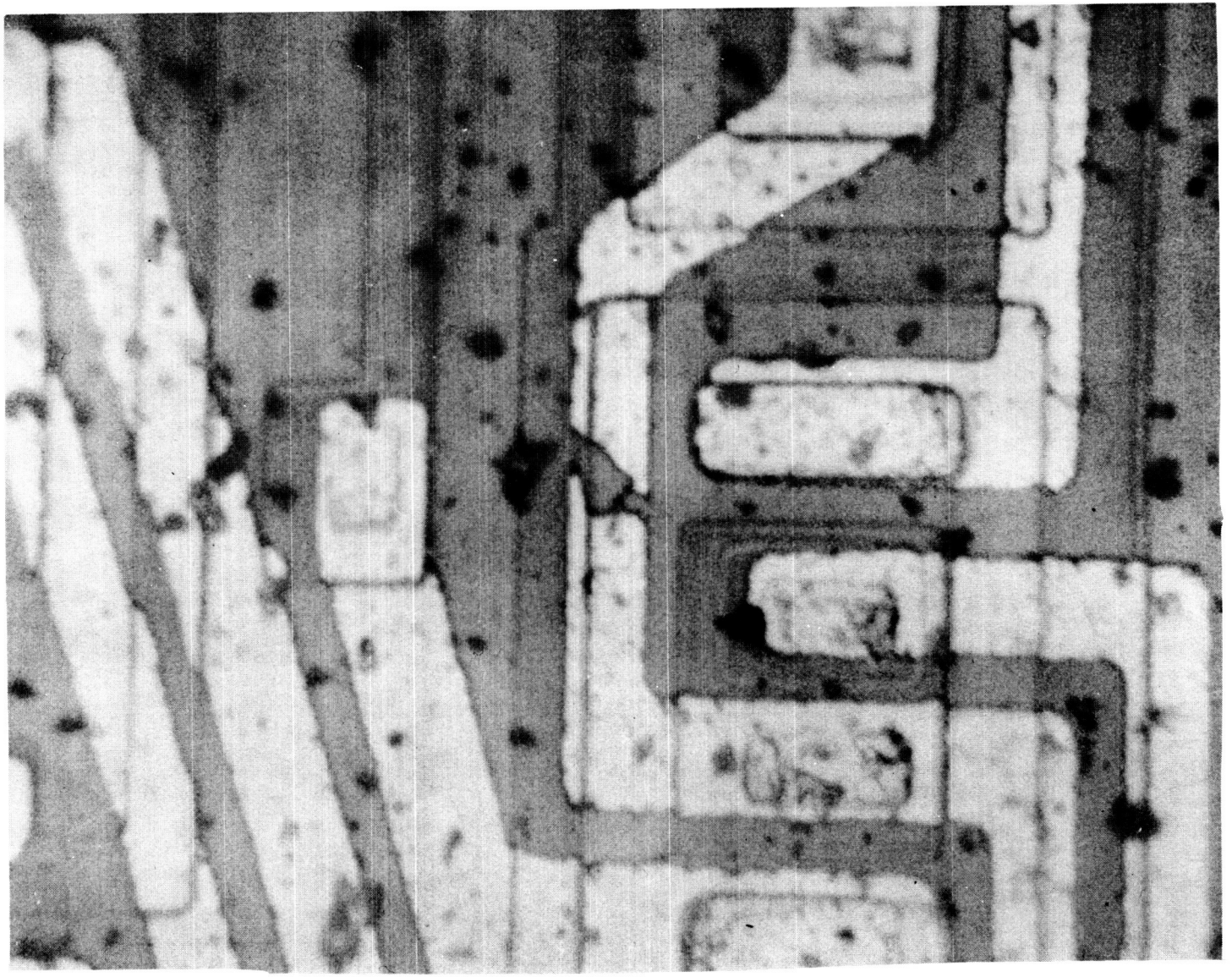

Figure 20. Aluminum Lead Damaged by Etchant

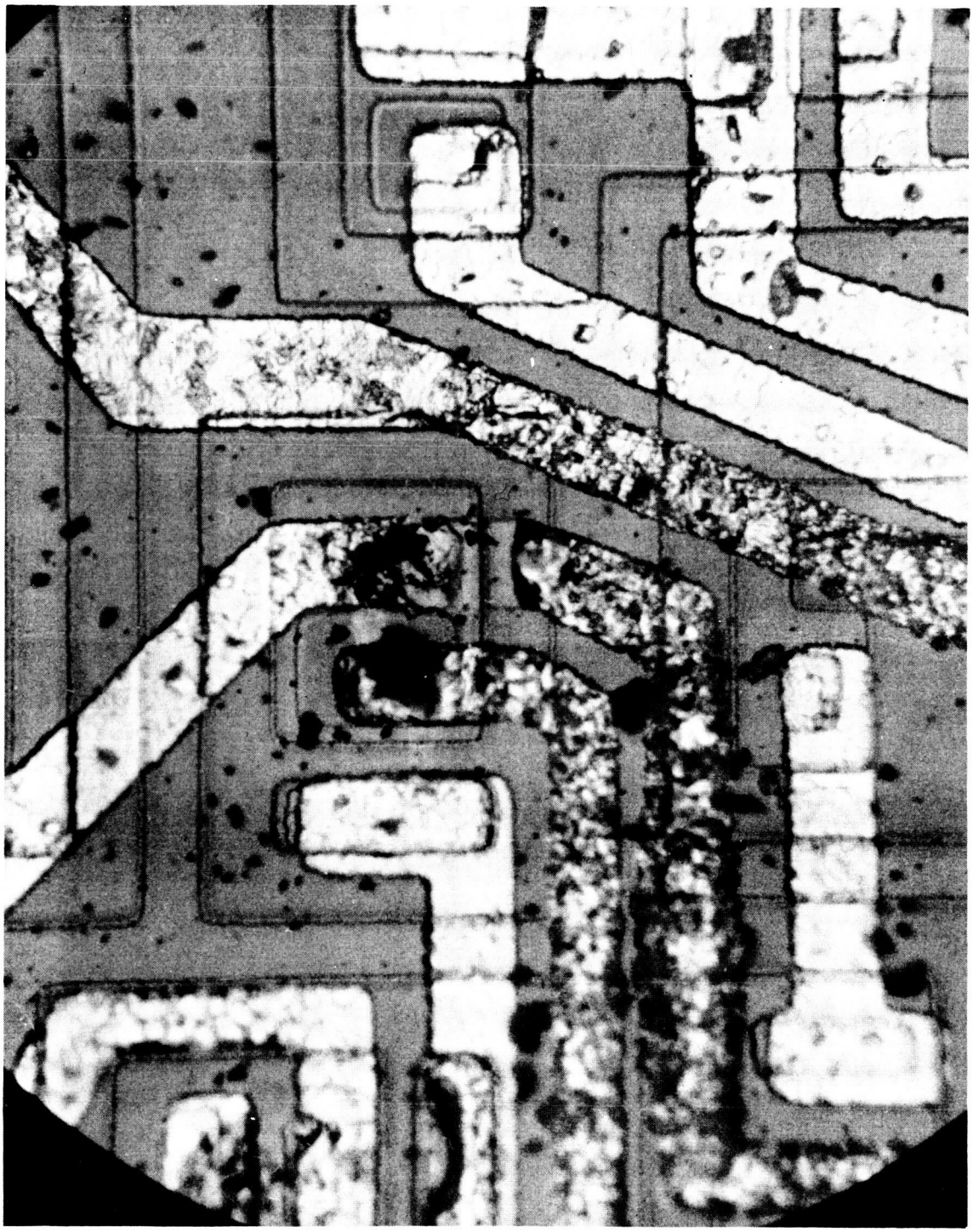

Figure 21. Chemical Reaction on Aluminum

November 21, 1966 NASA TM X-53548

APPROVAL

INVESTIGATIONS OF MONOLITHIC INTEGRATED CIRCUIT FAILURES

By

Kenneth W. Woodis

The information in this report has been reviewed for security classification. Review of any information concerning Department of Defense or Atomic Energy Commission programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

This document has also been reviewed and approved for technical accuracy.

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